Z86E04/E08 SL1866

CMOS Z8® OTP MICROCONTROLLER

FEATURES

Part Number	ROM (Kbytes)	RAM* (Bytes)	Speed (MHz)
Z86E08	2	125	12
Z86E04	1	125	8

* General-Purpose

- 18-Pin DIP and SOIC Packages
- 3.0- to 5.5-Volt @ 0°C to 70°C
- 14 Input / Output Lines
- Six Vectored, Prioritized Interupts with Programmable Polarity
- Two Analog Comparators
- Program Options:
  - Low Noise
  - ROM Protect
  - Auto Latch
  - Watch-Dog Timer (WDT)
- Two Programmable 8-Bit Counter/Timers, Each wth 6-Bit Programmable Prescaler
- WDT/ Power-On Reset (POR)
- On-Chip Oscillator that Accepts XTAL, Ceramic Resonance, LC, or External Clock
- Clock-Free WDT Reset
- Low-Power Consumption (50mw)
- Fast Instruction Pointer (1µs @ 12 MHz)

GENERAL DESCRIPTION

Zilog's Z86E04/E08 Microcontrollers (MCU) are One-Time Programmable (OTP) members of the Z8® single-chip microcontroller family which allow easy software development, debug, prototyping, and small production runs not economically desirable with masked ROM versions.

For applications demanding powerful I/O capabilities, the Z86E04/E08's dedicated input and output lines are grouped into three ports, and are configurable under software control to provide timing, status signals, or parallel I/O.

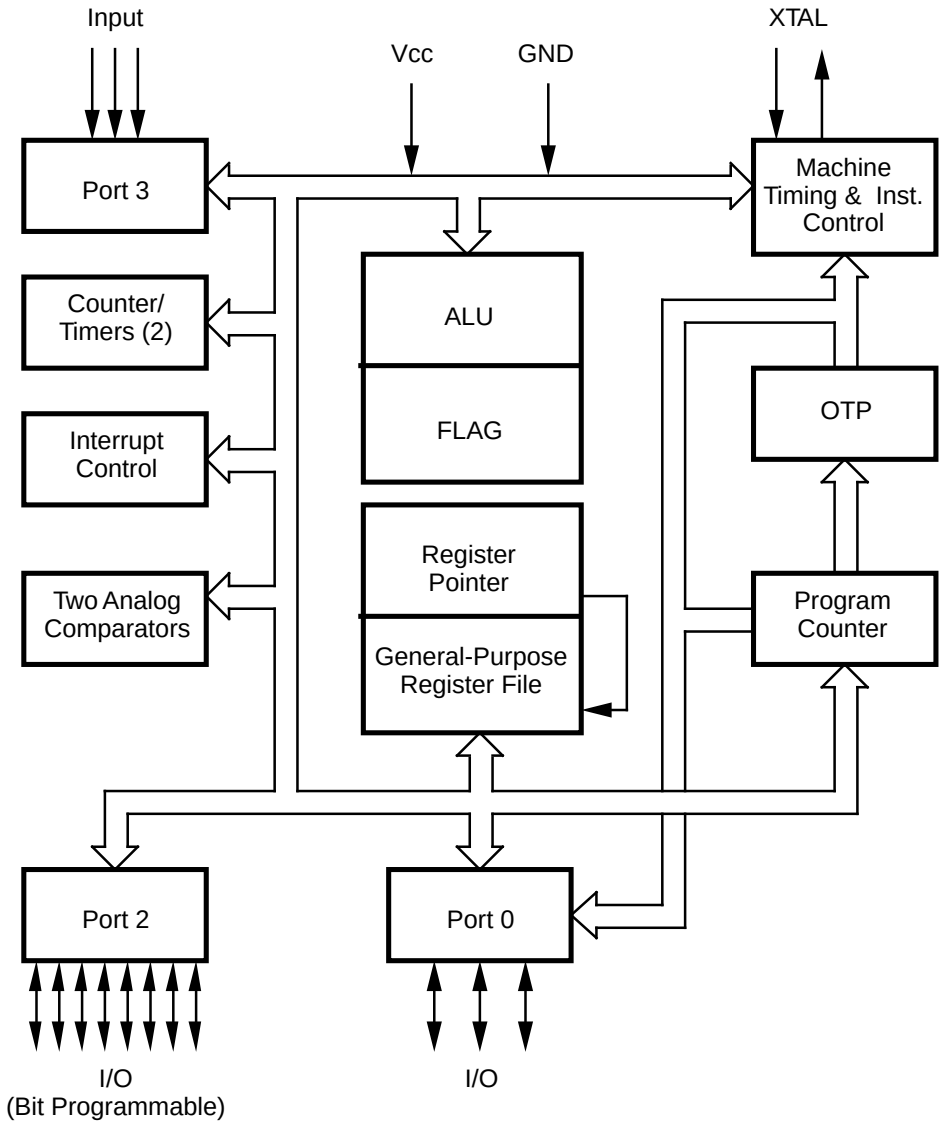
Two on-chip counter/timers, with a large number of user selectable modes, offload the system of administering real-time tasks such as counting/timing and I/O data communications.

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B/ /W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

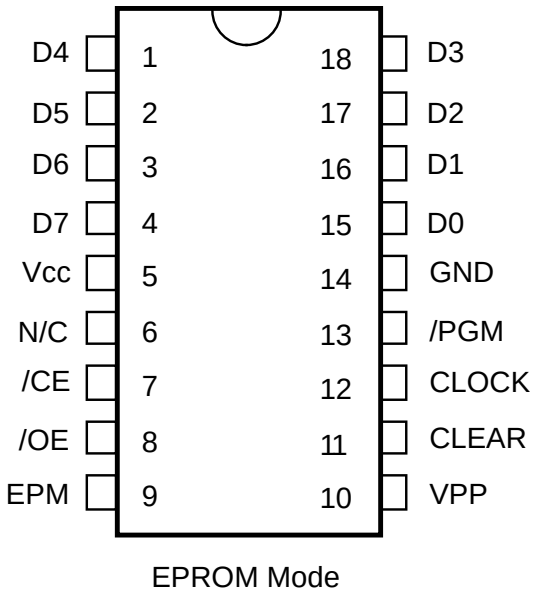
Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION (Continued)

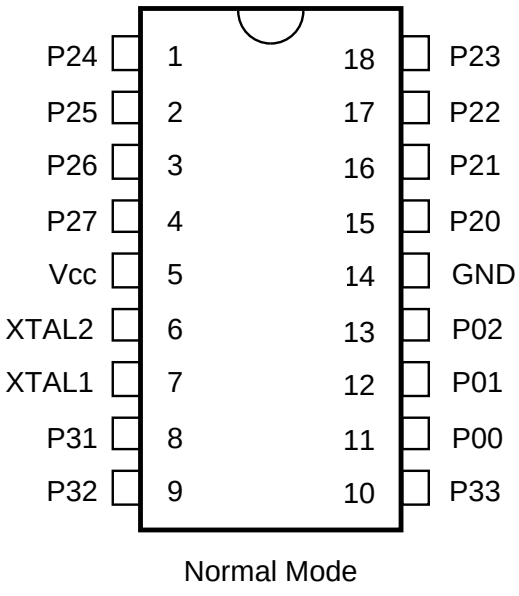


Functional Block Diagram

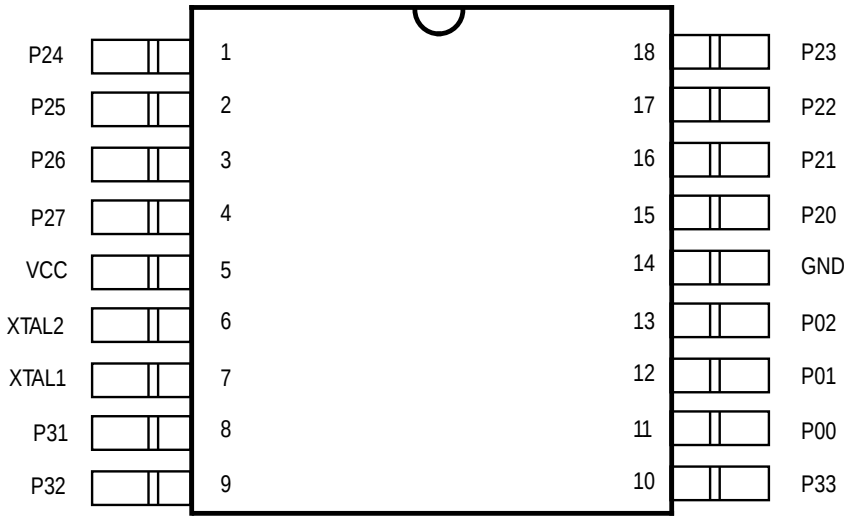
PIN DESCRIPTION



18-Pin EPROM Mode Configuration



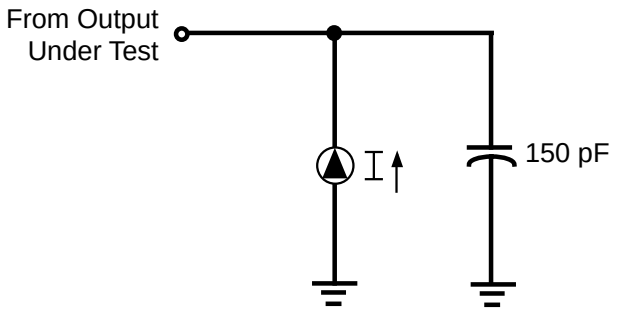
18-Pin Standard Mode Configuration



18-Pin SOIC Configuration

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load Diagram).



Test Load Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage*	-0.3	+7	V
T_{STG}	Storage Temp	-65	+150	°C
T_A	Oper Ambient Temp	†	†	°C

Notes:
* Voltages on all pins with respect to GND.
† See Ordering Information

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f =1.0 MHz, unmeasured pins to GND.

Parameter	Max
Input Capacitance	10 pF
Output Capacitance	20 pF
I/O Capacitance	25 pF

V_{CC} SPECIFICATION

3.0-V to 5.5-V @ 0°C to 70°C

PRODUCT RECOMMENDATIONS

Zilog recommends the following programming equipment for use with this One-Time Programmable product:

Device Type	Zilog Support Tool	Revision Level Software
Z86E08	Z86CCP00ZEM	3.0

Some non-Zilog programmers may have different programming waveforms, voltages and timings and not all programmers may meet the programming requirements of Zilog's One-Time Programmable products.

If difficulty is encountered in programming a Zilog OTP product, please contact your local Zilog sales office.

DC ELECTRICAL CHARACTERISTICS

Sym	Parameter	V_{CC} [4]	T_A = 0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
	Max Input Voltage	4.5V		12		V	I_{In} <250µA	
		5.5V		12		V	I_{In} <250µA	
V_{CH}	Clock Input High Voltage	4.5V	0.8V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
		5.5V	0.8V_{CC}	V_{CC}+0.3	2.8	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	4.5V	V_{SS}–0.3	0.2V_{CC}	1.7	V	Driven by External Clock Generator	
		5.5V	V_{SS}–0.3	0.2V_{CC}	1.7	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	4.5V	0.7V_{CC}	V_{CC}+0.3	2.8	V		
		5.5V	0.7V_{CC}	V_{CC}+0.3	2.8	V		
V_{IL}	Input Low Voltage	4.5V	V_{SS}–0.3	0.2V_{CC}	1.5	V		
		5.5V	V_{SS}–0.3	0.2V_{CC}	1.5	V		
V_{OH}	Output High Voltage	4.5V	V_{CC}–0.4		4.8	V	I_{OH} =–2.0mA	[5]
		5.5V	V_{CC}–0.4		4.8	V	I_{OH} =–2.0mA	[5]
		4.5V	V_{CC}–0.4		4.8	V	Low Noise@I_{OH} =–0.5mA	
		5.5V	V_{CC}–0.4		4.8	V	Low Noise@I_{OH} =–0.5mA	
V_{OL1}	Output Low Voltage	4.5V		0.4	0.1	V	I_{OL} =+4.0 mA	[5]
		5.5V		0.4	0.1	V	I_{OL} =+4.0 mA	[5]
		4.5V		0.4	0.1	V	Low Noise@I_{OL} =1.0mA	
		5.5V		0.4	0.1	V	Low Noise@I_{OL} =1.0mA	
V_{OL2}	Output Low Voltage	4.5V		1.0	0.8	V	I_{OL} =+12mA,	[5]
		5.5V		0.8	0.8	V	I_{OL} =+12mA,	[5]
V_{OFFSET}	Comparator Input Offset Voltage	4.5V		25	10	mV		
		5.5V		25	10	mV		
V_{RST}	V_{CC} Low Voltage Auto Reset		2.6	2.8	3.0	V	@6MHz Max, Int. CLK Freq	
I_{IL}	Input Leakage (Input Bias Current of Comparator)	4.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
I_{OL}	Output Leakage	4.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
		5.5V	–1.0	1.0		µA	V_{IN}=OV,V_{CC}	
V_{VCR}	Comparator Input Common Mode Voltage Range		0	V_{CC}–1.0		V		

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC}[4]	T_A=0°C to +70°C Min	Max	Typical @25°C	Units	Conditions	Notes
I_{CC}	Supply Current	4.5V		11.0	6.8	mA	All Output and I/O Pins Floating @2MHz	[5]
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @2MHz	[5]
		4.5V		15.0	8.2	mA	All Output and I/O Pins Floating @8MHz	[5]
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @8MHz	[5]
		3.0V		20.0	12.0	mA	All Output and I/O Pins Floating @12MHz	[5,6]
		5.5V		20.0	12.0	mA	All Output and I/O Pins Floating @12MHz	[5,6]
I_{CC1}	Standby Current	3.0V		4.0	2.5	mA	HALT mode V_{IN}=0V, V_{CC} @2MHz	[5]
		5.5V		4.0	2.5	mA	HALT mode V_{IN}=0V, V_{CC} @2MHz	[5]
		3.0V		5.0	3.0	mA	HALT mode V_{IN}=OV, V_{CC} @8MHz	[5]
		5.5V		5.0	3.0	mA	HALT mode V_{IN}=OV, V_{CC} @8MHz	[5]
		3.0V		7.0	4.0	mA	HALT mode V_{IN}=OV, V_{CC} @12MHz	[5,6]
		5.5V		7.0	4.0	mA	HALT mode V_{IN}=OV, V_{CC} @12MHz	[5,6]
I_{CC}	Supply Current (Low Noise Mode)	3.0V		11.0	6.8	mA	All Output and I/O Pins Floating @1MHz	
		5.5V		11.0	6.8	mA	All Output and I/O Pins Floating @1MHz	
		3.0V		13.0	7.5	mA	All Output and I/O Pins Floating @2MHz	
		5.5V		13.0	7.5	mA	All Output and I/O Pins Floating @2MHz	
		3.0V		15.0	8.2	mA	All Output and I/O Pins Floating @4MHz	
		5.5V		15.0	8.2	mA	All Output and I/O Pins Floating @4MHz	

DC ELECTRICAL CHARACTERISTICS (Continued)

Sym	Parameter	V_{CC} [4]	T_A=0°C to +70°C Min	Max	Typical @25°C	Units	Conditions
I_{CC1}	Standby Current (Low Noise Mode)	4.5V		1.6	0.9	mA	HALT mode V_{IN}=0V, V_{CC}@1MHz
		5.5V		1.6	0.9	mA	HALT mode V_{IN}=0V, V_{CC}@1MHz
		4.5V		1.9	1	mA	HALT mode V_{IN}=0V, V_{CC}@2MHz
		5.5V		1.9	1	mA	HALT mode V_{IN}=0V, V_{CC}@2MHz
		4.5V		2.4	1./5	mA	HALT mode V_{IN}=0V, V_{CC}@4MHz
		5.5V		2.4	1.5	mA	HALT mode V_{IN}=0V, V_{CC}@4MHz
I_{CC2}	Standby Current	4.5V		10	1.0	µA	STOP mode V_{IN}=OV, V_{CC} WDT is not Running
		5.5V		10	1.0	µA	STOP mode V_{IN}=OV, V_{CC} WDT is not Running
I_{ALL}	Auto Latch Low Current	4.5V		32	16	µA	$OV<V_{IN}<V_{CC}$
		5.5V		32	16	µA	$OV<V_{IN}<V_{CC}$
I_{ALH}	Auto Latch High Current	4.5V		–25	-8.0	µA	$OV<V_{IN}<V_{CC}$
		5.5V		–25	-8.0	µA	$OV<V_{IN}<V_{CC}$

Notes:

[1] Port 2 and Port 0 only.

[2] V_{SS} = 0V = GND

[3] The device operates down to V_{RST}. of the specified frequency for V_{RST} The minimum operational V_{CC} is determined on the value of the voltage V_{RST} at the ambient temperature. The V_{RST} increases as the temperature decreases.

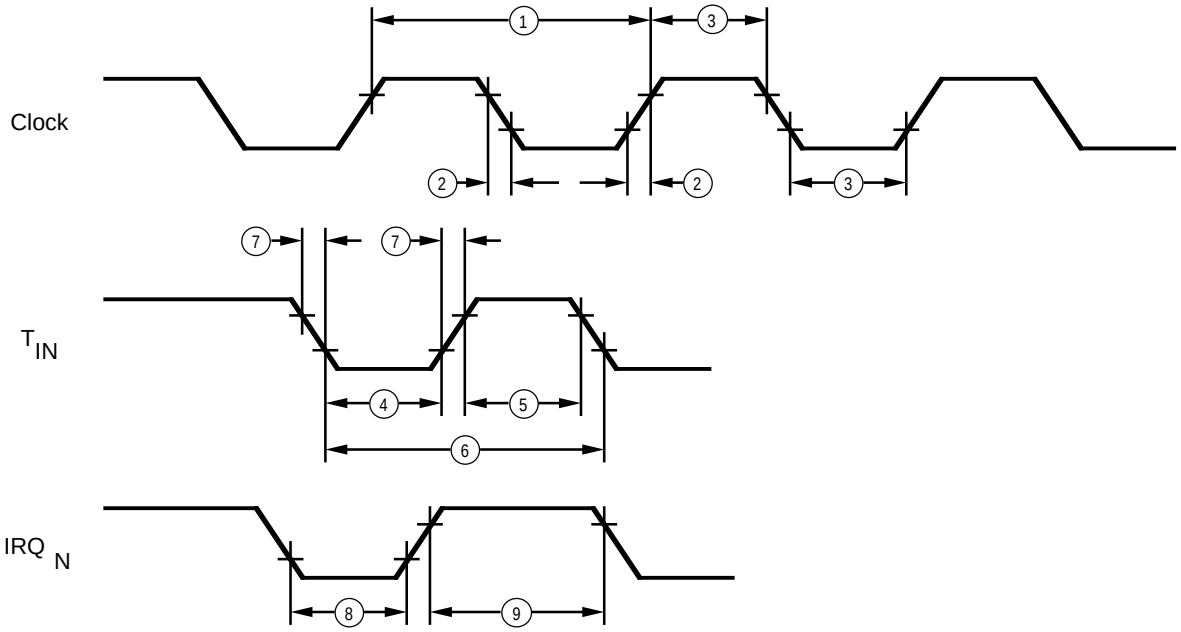
[4] V_{CC} = 3.0V to 5.5V, typical values measured at V_{CC} = 3.3V and V_{CC} = 5.0V.

[5] Standard Mode (not Low EMI mode)

[6] Z86E08 only.

[7] CL1 = 100 pF, CL2 = 220 pF, RF = 30 kOhm

AC ELECTRICAL CHARACTERISTICS



AC Electrical Timing Diagram

AC ELECTRICAL CHARACTERISTICS

Timing Table (Standard Mode for SCLK/TCLK = XTAL/2)

				T_A=0°C to +70°C 8MHz(C04)		12MHz(C08)			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TpC	Input Clock Period	4.5V	125	DC	83	DC	ns	[1]
			5.5V	125	DC	83	DC	ns	[1]
2	TrC,TfC	Clock Input Rise	4.5V		25		15	ns	[1]
		and Fall Times	5.5V		25		15	ns	
3	TwC	Input Clock Width	4.5V	62		41			[1]
			5.5V	62		41		ns	[1]
4	TwTinL	Timer Input Low Width	3.0V	70		70		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.0V	5TpC		5TpC		[1]	
			5.5V	5TpC		5TpC		[1]	
6	TpTin	Timer Input Period	3.0V	8TpC		8TpC			[1]
			5.5V	8TpC		8TpC			[1]
7	TrTin,	Timer Input Rise	3.0V		100		100	ns	[1]
	TfTin	and Fall Timer	5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input	3.0V	70		70		ns	[1,2]
		Low Time	5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input	3.0V	5TpC		5TpC			[1]
		High Time	5.5V	5TpC		5TpC			[1,2]
10	Twdt	Watch-Dog Timer	3.0V	12		12		ms	[1]
		Delay Time for Timeout	5.5V	12		12		ms	[1]
11	Tpor	Power-On Reset Time	3.0V	12		12		ms	[1]
			5.5V	12		12		ms	[1]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

AC ELECTRICAL CHARACTERISTICS

Low Noise Mode

				T_A=0°C to +70°C					
				1MHz		4MHz			
No	Symbol	Parameter	V_{CC}	Min	Max	Min	Max	Units	Notes
1	TPC	Input Clock Period	4.5V	1000	DC	250	DC	ns	[1]
			5.5V	1000	DC	250	DC	ns	[1]
2	TiC	Clock Input Rise	4.5V		25		25	ns	[1]
	TfC	and Fall Times	5.5V		25		25	ns	[1]
3	TwC	Input Clock Width	4.5V	500		125		ns	[1]
			5.5V	500		125		ns	[1]
4.	TwTinL	Timer Input Low Width	4.5V	70		70		ns	[1]
			5.5V	70		70		ns	[1]
5	TwTinH	Timer Input High Width	4.5V	2.5TpC		2.5TpC			[1]
			5.5V	2.5TpC		2.5TpC			[1]
6	TpTin	Timer Input Period	4.5V	4TpC		4TpC			[1]
			5.5V	4TpC		4TpC			[1]
7	TrTin,	Timer Input Rise	4.5V		100		100	ns	[1]
	TfTin	and Fall Timer	5.5V		100		100	ns	[1]
8	TwIL	Int. Request Input	4.5V	70		70		ns	[1,2]
		Low Time	5.5V	70		70		ns	[1,2]
9	TwIH	Int. Request Input	4.5V	2.5TpC		2.5TpC			[1]
		High Time	5.5V	2.5TpC		2.5TpC			[1,2]
10	Twdt	Watch-Dog Timer	4.5V	12		12		ms	[1]
		Delay Time for Timeout	5.5V	12		12		ms	[1]

Notes:

[1] Timing Reference uses 0.7 V_{CC} for a logic 1 and 0.2 V_{CC} for a logic 0.

[2] Interrupt request through Port 3 (P33-P31).

PRECAUTIONS

1) ROM Protect does not automatically enable the Low EMI Mode.

Low Margin:
Customer is advised that this product does not meet Zilog's internal guardbanded test policies for the specification requested and is supplied on an exception basis. Customer is cautioned that delivery may be uncertain and that, in addition to all other limitations on Zilog liability stated on the front and back of the acknowledgement, Zilog makes no claim as to quality and reliability under the CPS. The product remains subject to standard warranty for replacement due to defects in materials and workmanship.

Pre-Characterization Product:
The product represented by this CPS is newly introduced and Zilog has not completed the full characterization of the product. The CPS states what Zilog knows about this product at this time, but additional features or non-conformance with some aspects of the CPS may be found, either by Zilog or its customers in the course of further application and characterization work. In addition, Zilog cautions that delivery may be uncertain at times, due to start-up yield issues.

Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com